

Remarks

The various parts of the Office Action (and other matters, if any) are discussed below under appropriate headings.

Oath/Declaration

The Examiner has objected to the declaration on the basis it appears to be post dated. The Examiner is advised the date on the declaration is in European format (day/month/year), and thus the declaration was signed on September 11, 2003 and not November 9, 2003.

Drawings

The drawing sheet containing Figure 1 has been objected to for not being labeled as "Prior Art." Enclosed is a replacement drawing sheet wherein the legend "Prior Art" has been added to Figure 1.

Specification

The Abstract has been objected to because it contains more than 150 words. The Abstract has been amended to reduce the word count to no more than 150 words.

Claim Objections

Claims 6-8 and 9-10 has been objected to because of several informalities. The changes suggested by the Examiner have been made.

Claim Rejections - 35 USC § 103

Claim 1 has been amended to include the feature of claim 2, and claim 17 has been amended to include the feature of claim 18. Consequently, the rejection of claims 1, 11-16 and 17 is now moot.

Claims 2 and 18 were rejected as being unpatentable over Bedingfield et al. (US 5,537,654) in view of Applicant Admitted Prior Art (Specification - page 1, line 21

through page 3, line 11 and Fig. 1) and Moss et al. (US 5,604,870). In particular, the Examiner stated that although the combination of Bedingfield et al. and AAPA (which is used to reject claim 1) does not disclose the claim 2 feature of the parallel interface operating under control of the register set, this feature is disclosed in Moss et al., and it would be obvious to modify Bedingfield et al. to include it. As will become apparent from the following discussion, the combination advanced by the Examiner does not yield the subject matter of claim 2 (now amended claim 1).

Bedingfield et al. describes a peripheral device with a shared memory region accessible to both a host computer and a CPU in the device. Boot information may thus be transferred from the host computer to a program memory of the peripheral device via the shared memory. This allows the operating program of the peripheral device to be updated by the host computer, e.g. to fix bugs and so on, after manufacture. As an aside, Bedingfield notes that the shared memory can also be used to transfer data from the host to the peripheral device directly (column 7, lines 10 to 27). This is done by dedicating a portion of the shared memory as a buffer for transferring data from the CPU to the peripheral device (column 7, lines 25 to 27).

Moss et al. describes a device designed to emulate a UART. The emulated UART is designed to provide the "look and feel" of a conventional UART. Thus Moss et al. includes features corresponding to those of a normal UART. Moss et al. is designed to emulate a wholly conventional UART, even to the extent that it purposely slows itself down to match the timing limitations of a conventional UART, e.g. see column 6, lines 48 to 53 and column 7, lines 11 to 15. Moss et al. does not describe anything that could be considered a parallel interface configurable to establish an auxiliary parallel data communication channel operable in conjunction with the serial data channel, as recited in amended claim 1. Accordingly, and contrary to what is stated in the Office Action, Moss et al. also does not disclose operating such a parallel interface under control of the UART register set, also as recited in amended claim 1.

In section 13 of the Office Action the Examiner comments further on Moss et al. in connection with some other claims. From the comments made in this section it appears that the Examiner considers the data buffers 221 and 223 in Figure 2 of Moss et al. to be associated with an auxiliary parallel data communication channel. However, there is no auxiliary parallel data communication channel in Moss et al. The data buffers 221 and 223 merely correspond to the FIFO data buffers used in a conventional UART (i.e. elements 24 and 26 in the UART described in AAPA). For example, see column 3, lines 54 to 59 of Moss et al.

Thus none of the cited documents disclose or suggest an auxiliary parallel interface operating under control of the UART register set. Even if Moss et al. were to disclose an auxiliary parallel interface operating under control of the UART register set (which it does not), this feature is technically incompatible with Bedingfield et al. In Bedingfield et al., the shared memory is used for transferring data directly from the CPU to the peripheral device (column 7, lines 25 to 27). It is an important requirement in Bedingfield et al. that the transfer is direct and independent of the UART functioning (i.e. not under the control of the UART registers). This is because the host computer must be able to access the shared memory when the peripheral device is in a non-functioning state in order that the program memory of the peripheral device may be overwritten.

A number of advantages are associated with having the parallel data communication channel operate under control of the UART registers. For example, the device can be configured so that UART device drivers can operate in a default mode without any modification, i.e. the UART behaves as-normal at first inspection. An enhanced driver, however, can activate the parallel channel through the conventional UART register(s) which control it to take advantage of faster transfer rates. Thus a way to add an enhanced capability to an existing UART architecture is provided which retains full backward compatibility. The choice of whether to use the UART in the "normal" or "enhanced" mode is up to the designer who wants to use the UART. A

designer can make this choice safe in the knowledge that he can run with the standard drivers for the normal mode, and use an enhanced driver to access the enhanced modes without encountering compatibility problems.

For at least the foregoing reasons, the rejection of the claims should be withdrawn.

Conclusion

In view of the foregoing, request is made for timely issuance of a notice of allowance.

Respectfully submitted,

RENNER, OTTO, BOISSELLE & SKLAR, LLP

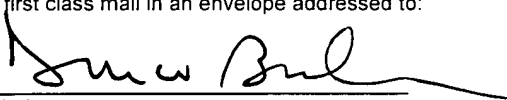
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CERTIFICATE OF MAILING (37 CFR 1.8a)

I hereby certify that this paper (along with any paper or thing referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date: November 10, 2005


Don W. Bulson

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Amendments to the Drawings

The attached replacement sheet(s) of drawings replace(s) the sheets with the corresponding figures. The replacement sheets include the following changes:

The legend "Prior Art" has been added to Figure 1.